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S P E C I F I C A T I O N

1. Title of the Invention

Gas Phase Reaction Coat Manufacturing Apparatus and Manufacturing Method

2. Claim

1. A vapor phase reaction film manufacturing apparatus, in a reactor for performing vapor phase reduced pressure, comprising: means for supplying reactive gas; reaction vessel means to which thermal energy, light energy and electric energy, or energy jointly using the above for manufacturing said reactive gas on a formed surface; means for discharging undesired reactive gas and undesired reaction product in said reaction vessel; and means for exhausting evacuating or pressure reducing means through a pressure regulating valve, and a turbo-molecular pump by a rotary pump and a mechanical booster pump or the

like.

2. A vapor phase reaction film manufacturing method, wherein in a reactor for performing gas reaction under reduced pressure, under the coat forming conditions by reaction in a reaction vessel using a gas phase reactor comprising means for supplying reactive gas; reaction vessel means to which thermal energy, light energy and electric energy, or energy jointly using the above for manufacturing said reactive gas on a formed surface; means for discharging undesired reactive gas and undesired reaction product in said reaction vessel; and means for exhausting evacuating or pressure reducing means through a pressure regulating valve, and a turbo-molecular pump by a rotary pump and a mechanical booster pump or the like, the interior of said reaction vessel is kept in the region of 0.05~10torr, and under said pressure regulating valve, 10^{-2}torr or less is kept to perform film formation.

3. Detailed Description of the Invention

This invention relates to gas phase reaction film manufacturing apparatus and manufacturing method. This invention relates to manufacturing a film of a non-oxide at the time of manufacturing a film by use of reactive gas, and the gas reactor and its manufacturing method by which the concentration with the mixing amount of oxygen in a film of

$1\times10^{19}cm^{-3}$ is obtained by performing gas reaction (hereinafter referred to as CVD) by use of a turbo-molecular pump in the exhaust system.

This invention is characterized in that in manufacturing a non-oxide film, in order to prevent counterflow of atmospheric air from its exhaust system, not only a discontinuously rotation type vacuum pump (hereinafter referred to as vacuum pump or VP simply) such as an oil-sealed rotary vacuum pump, a mechanical booster pump or the like, but also a continuously exhaust type turbo-molecular pump (hereinafter referred to as turbo-molecular pump or TP simply) is interposed between a reaction vessel and a vacuum pump to prevent counterflow of atmospheric air from the exhaust system.

At the time of forming a non-oxide film of the present invention, for example, non-single crystal silicon by use of silane (Si_nH_{2n+2} $n\geq1$) which is reactive gas, it is an object of the invention to prevent counterflow from the exhaust system in order that the quantity of oxygen in the film is $5\times10^{18}cm^{-3}$ or less, preferably $1\times10^{18}cm^{-3}$ or less.

According to the present invention, such exhaust system is so constructed that TP is interposed between a reaction chamber and VP through a pressure regulating valve in process of reaction, whereby with the interior of the

reaction chamber kept in the pressure range of 0.05~10torr, film formation is performed by plasma CVD method (called PVCD), photo-chemical vapor deposition (Photo CVD) method, or a method jointly using the above (hereinafter referred to as CVD method simply), and under the pressure regulating valve, pressure of 1×10^{-2} or less (generally 10^{-4} ~ 10^{-6}torr) is kept, and in order to operation TP, the system of reaction is kept with pressure (1×10^{2}torr or more, that is, 0.05~10torr) higher than that of the exhaust system to perform film formation. This is an object of the present invention.

Further the present invention relates to a manufacturing method for a semiconductor device in which the plasma CVD device has plural reaction chambers connected to each other, and in the respective reaction chambers, a P-type non-single crystal semiconductor, an I-type non-single crystal semiconductor and an N-type non-single crystal semiconductor are stacked on a substrate to construct PIN junction.

Conventionally, in the CVD device, for example, in the PCVD device, the pressure of the reaction system is high, 0.05~10torr, so that the exhaust system or the like uses VP only, and it is quite impossible to provide TP or the like for generating vacuum of a degree above that.

However, the inventor of the present invention has found

that in such a PCVD device, if the exhaust system uses a VP only, the VP makes discontinuous rotary motion, so that the atmospheric air (especially oxygen) from the exhaust system with the atmospheric pressure which comes into contact with the air flows backward, and further some of the atmospheric air gets mixed in the oil and is again vaporized to flow backward into a reaction vessel.

Further, it thus gets mixed in a film formed by oxygen due to such a couterflow, and for example, in the case of manufacturing a silicon film, oxygen got mixed in the film with the concentration of 3×10^{19} ~ $2\times10^{20}cm^{-3}$.

Thus, hydrogen or fluorine is added to such a film so that the film becomes low-grade silicon oxide, though it should be a silicon semiconductor.

It is an object of the invention to prevent such disadvantages.

Figure 1 shows the outline of an apparatus according to the present invention. That is, the apparatus comprises a doping system 50 for introducing reactive gas, a reaction vessel 51, and an exhaust system 52. When the reaction vessel is of such a double reaction vessel type as to have a reaction space inside, the inner surface of which is formed of an insulating material to form a semiconductor layer, and further additionally a P-type semiconductor (system I in the

drawing), an I-type semiconductor (system II in the drawing), and an N-type semiconductor are stacked to form a junction on a substrate, the respective reaction vessels are connected to each other through a separating part (system II in the drawing). Such a multi-chamber system PCVD method has been proposed as shown in Figure 1.

This invention relates to plasma vapor phase reaction for conducting continuous production, in which a semiconductor layer having P, I and N type conductive types with a smaller recombination center density is formed by formation of a non-single crystal semiconductor layer to which hydrogen or halogen elements are added, and PIN junction is formed in the lamination layer boundary, whereby impurities from the other adjacent semiconductor layer can be prevented from mixing in the respective semiconductor layer to deteriorate junction characteristics, and further during the processes of forming the respective semiconductor layers, they can be prevented from coming into contact with the atmospheric air, especially oxygen to oxidize a part of the semiconductor and form a layer insulating material.

Further this invention relates to the so-called mass-production system, in which in a multi-chamber system plasma reaction method having many such reaction vessels connected to each other in such a manner as to be independent in each reaction, many substrates are simultaneously increased in

its film growth speed at one time.

In this invention, used is a substrate with dimensions of 10cm×10cm, or 10~50cm in the direction of an electrode, for example, 40cm, and a width of 15~120cm, for example, 60cm (20 sheets of patches with dimensions of 40cm×60cm or 20cm×60cm are arranged).

In Figures 1 and 2, the apparatus has introducing means for reactive gas and exhaust means which are provided with a supply nozzle and an exhaust nozzle, and a pair of electrodes 61, 51 or 62, 52; reactive gas supply nozzles 17, 18, and exhaust nozzles 17', 18' are arranged inside of an insulating hood. That is, structures 39, 39' are such that the outside of the electrode is enclosed with an insulating material of the hood. Further, in order to confine the reaction space between the hoods, the periphery of the outside is surrounded with insulating materials 38, 38'.

Figure 2 is a section of Figure 1, in which opening and closing doors are provided in front (left side in the drawing) and in rear (right side in the drawing) of a reaction vessel, and heating means 13, 13' comprising a halogen lamp or the like are provided on the inner surfaces of the doors.

The embodiment of the invention will now be described

with reference to the attached drawings.

Embodiment 1

An embodiment of a plasma vapor phase reactor according to the present invention will be described with reference to Figures 1 and 2.

The drawings show an apparatus for forming in multi-layer, automatically and continuously a semiconductor layer which is dissimilar conductive type and different in principal component or stoichiometric ratio of a formed semiconductor on a semiconductor on a substrate of PIN junction, PIP junction, NIN junction or PINPIN.. PIN junction or the like, to stack the respective semiconductor layers without any influence (mixing-in) of a semiconductor layer formed in the preceding process.

The drawings show a part of plural reaction systems for constructing PIN junction. That is, the drawings show an example of a multi-chamber type plasma vapor phase reactor having two (I, II) of three reaction systems for forming P, I and N type semiconductor layers in the stacking state and further a first spare chamber and a buffer chamber II (for transferring).

In the drawings, the systems I, II, III respectively comprise two reaction vessels 101, 103 and a buffer chamber 102, wherein separation parts 44, 45, 46, 47 are provided between the respective reaction vessels. Further,

independently supply nozzles 17, 18 for reactive gas and exhaust nozzles 17', 18' are provided to form a laminar flow of reactive gas from the supply system to the exhaust system.

The apparatus is provided with a first preliminary chamber 100 on the inlet side, and first two substrates 1 having two formed surfaces are inserted in two faces of a substrate holder 2 from a door 42. Further, holders 3 are arranged at spaces of a designated equal distance by an enclosure jig (only outer circumference is shown as 38, 38'). That is, the substrate having the formed surfaces is disposed in such a manner that the back where film formation is not performed is brought into contact with the substrate holder 2, and two substrates and the substrate holder are taken as one holder 3 to stand together in large numbers at intervals of 6cm ± 0.5cm in the enclosure jig of an insulating material. As a result, film formation could be performed on 20 sheets of substrates with dimensions of 40cm×60cm at the same time. Thus, the reaction spaces (6, 8) 55cm in height, 80cm in depth and 80cm in width are surrounded on the upper side and the lower side with insulating materials 39, 39', and the side circumference is surrounded with insulating enclosure jigs 38, 38'.

With a pressure regulating valve 71 fully opened, a

first preliminary chamber 100 is evacuated through a TP 86 by a vacuum pump 35. After that, the pressure regulating vale 72 is totally opened, and a gate valve 44 for separation from a reaction vessel 101 previously evacuated to 3×10^{-8}torr or less by the TP is opened to transfer the substrate held on the enclosure jig 38. For example, the substrate is transferred from the preliminary chamber 100 to the first reaction vessel 101, and further the gate valve 44 is closed to move the substrate to the first reaction vessel 101. At this time, the substrate 1 or the like held in the first reaction vessel 101 can be previously or simultaneously moved to a buffer chamber 102, the jig and the substrate 2 held in the buffer chamber 102 can be moved to a second reaction vessel 103, the substrate held in the second reaction vessel 103 can be moved to a second buffer chamber 104, and further not being shown, the substrate and the jig in the third reaction vessel can be moved to a second preliminary chamber by opening the gate valves 45, 46, 47. After that, the gate valves 44, 45, 46, 47 are closed.

That is, the gate valves are operated in such a manner that when a door 42 is opened by the atmospheric pressure, the gate valves 44, 45, 46, 47 of the separation parts are closed and in each chamber, plasma vapor phase reaction is

performed. On the contrary, when the door 42 is closed and the preliminary chamber 100 is enough evacuated, the gate valves 44, 45, 46, 47 are opened and the substrate and the jig in each chamber are moved to the adjacent chamber, so that the outside air is kept from getting mixed in the reaction chambers 101, 102.

The case of forming a P-type semiconductor layer in the first reaction vessel 101 in the system I by a PCVD method will be shown in the following.

The reaction system I (the reaction vessel 101 included) is 0.01 ~ 10torr, preferably 0.01 ~ 1torr, for example 0.08torr.

That is, with the pressure regulating valve closed, the pressure in the reaction vessel 101 is 0.05 ~ 1torr, and under the valve, it is 1×10^{-2}torr or less, generally 1×10^{-4} ~ 1×10^{-7}torr. This degree of vacuum is achieved by rotating the TP 87. Further, as the continuous exhaust system TP is operated, inverse diffusion of polymerized oil of the VP 36, and counterflow of exhaust atmospheric air, especially oxygen impregnated in oil could be prevented for the first time.

Reactive gas is supplied from the doping system 50 of the system I. That is, as silicide gas 24, used are silane (Si_nH_{2n+2}, $n\geq1$, especially SiH_4 or Si_2H_6) which is refined and

filled in a stainless cylinder and silicon fluoride (SiF_2 or SiF_4). In this case, used is ultra high purity silane (the purity is 99.99%, provided that water and oxygenation matter are 0.1 PPM or less) which is easy to handle.

In order to form the present embodiment of Si_xC_{1-x} ($0<x<1$), DMS (dimethyl silane $SiH_2(CH_3)_2$ the purity is 99.99%) is used as carbide gas 25.

For the silicon carbide (Si_xC_{1-x} $0<x<1$), as P-type impurity, boron is simultaneously mixed in the described monosilane with the concentration of 0.5% 24 to be supplied with silane.

At need, hydrogen (the purity is 7N or more) or nitrogen (the purity is 7N or more) is supplied from when the reaction chamber is the atmospheric pressure 23. Such reactive gas is passed through a flow meter 33 and a valve 32 and supplied from the supply nozzle 17 for reactive gas through a negative electrode 61 of a high-frequency power supply 14 to the reaction space.

The reactive gas is supplied to the interior of the cylindrical space 6 surround with the holder 38 to perform film formation on the substrate 1 for constructing the space. Further, electric energy, for example, high frequency energy 14 with a frequency of 13.56 MHz is applied between the negative electrode 61 and the positive electrode

51 to cause plasma reaction, thereby forming a film of reaction product on the substrate.

The substrate is heated to 100 ~ 400°C, for example 200°C by the same means as infrared heaters disposed in front and in rear of the vessel of the reaction vessel 103 shown in Figure 2.

The infrared heater uses a near infrared halogen lamp (light emission wavelength is 1 - 3μ) heater or a far infrared ceramic heater (light emission wavelength is 8 ~ 25 μ) , thereby setting the cylindrical space surrounded with the holder in the reaction vessel to 200 ± 10°C, preferably ±5°C.

After that, as described above, the described reactive gas is introduced into the vessel, and further high frequency energy 14 to 10 ~ 500, for example 100W is supplied to cause plasma reaction.

Thus, the P-type semiconductor layer is formed as a thin film with the average film thickness of 30 ~ 300Å, for example, a thickness of about 100Å by the reaction system I under the conditions of B_2H_6/SiH_4 = 0.5%, DMS/(SiH_4+DMS) = 10%. Eg = 2.05 eVσ = 1×10^{-6} ~ 3×10^{-5} $(\Omega cm)^{-1}$.

The substrate uses a conductor substrate (stainless, titanium, aluminium, other metals), a semiconductor (silicon, germanium), an insulator (glass, organic thin

film) or a composite substrate (two-layer film in which a conductive film of tin oxide, ITO or the like to which fluorine is added, which is a light transmitting conductive film is formed in single layer or ITO on glass or light transmitting organic resin). These are generally known as a substrate not only in the present embodiment, but in all of the present invention. Of course the substrate may be bending or a solid plate.

Thus, plasma vapor phase reaction is made for 1 ~ 5 minutes to manufacture a silicon carbide film to which boron is added as P-type impurity with a thickness of about 100Å. Further, the substrate where the first semiconductor layer is formed is moved to a buffer chamber 102 according to the described operation sequence by opening the gate 45, and the gate 45 is closed. The buffer chamber 102 is previously evacuated to 10^{-8}torr or less, for example 4×10^{-10}torr by a cryopump 88.

The substrate is transferred to the reaction vessel held to 1×10^{-7}torr or less by the TP 89 similarly to the system II through opening and closing of the gate 46.

That is, in the reaction system in Figure 1, as reactive gas of a semiconductor, ultra high purity monosilane or disilane (the concentration of water or silicon oxide and oxide gas is 0.1 PPM or less) from 28 or boron of $10^{17}cm^{-3}$ or

less is added, so that B_2H_6 diluted to 0.5 ~ 30PPM by hydrogen, silane or the like is supplied from 27, and further carrier gas is supplied at need from 26. Figure 3 is a longitudinal section taken from the outlet side in the system.

Outline of Figure 2 will be given.

Figure 2 is a longitudinal section of the reaction system of Figure 1.

In the drawing, the lamp heaters 13, 13' use a bar-like halogen lamp. The reaction space is heated to 100 ~ 400°C, for example 250°C by the heater.

The substrate 1 is held on the substrate holder 2, and confined by the enclosure jigs 38, 38' to form a space 8.

SiH_4 is 5000Å thick, 60cc/min. the film formation speed is 2.5Å/sec., the substrate (20 sheets with dimensions of 20cm×60cm, 24000cm^2 in total floor area), and the pressure is 0.1 torr. If Si_2H_6 is used, the film formation speed is 28Å/ sec.

Thus, an I-type semiconductor layer is formed on the P-type semiconductor layer formed by plasma vapor phase method in the first reaction chamber by PCVD method to construct PI junction.

After formation to a thickness of about 7000Å by the system, the substrate is moved to the adjacent buffer

chamber 102 according to the described operation, and further transferred to the adjacent reaction chamber to form a N-type semiconductor layer by the similar PCVD process. The N-type semiconductor layer is formed by the steps of forming a poly-crystal semiconductor layer having a N-type microcrystal property or fiber structure by supplying silane having phosphin PH_3/SiH_4 = 1.0% and hydrogen of carrier gas as SiH_4/H_2 = 20%, similarly to the system I to be about 200Å thick, and further stacking a N-type semiconductor layer shown by Si_xC_{1-x} ($0<x<1$) with silicon carbide of DMS/(SiH_4 + DMS) = 0.1 on the upper surface thereof to be 10 ~ 200Å thick, for example, 50Å thick. The others of the reactor are the same as those of the system I.

After such a process, ITO 100 ~ 1500Å thick is formed on the substrate having the PIN junction put out from a second preliminary chamber, and further reflective or sublimation metal electrode, for example, an aluminium electrode is made thereon about 1μ thick by a vacuum evaporation method to construct (ITO+SnO_2) surface electrode - (PIN semiconductor) - (back electrode) on the glass substrate.

The characteristic as the photoelectric transfer device has 7 ~ 9%, 8% on the average as intrinsic efficiency characteristic on the substrate of 10cm×10cm under the condition of AM1 (100mW/cm^2), and even on a glass substrate

of 40cm × 60cm, which is integrated to be of hybrid type, 5.5% can be obtained at the effective efficiency.

As a result, though the release voltage is 0.85 ~ 0.9V (0.87 ± 0.02V) at one element, short-circuit current is large, 18 ± 2 mA/cm^2, FF is large, 0.60 ~ 0.70, and its fluctuation is small in panel and a batch, from which it is found that the method of the present invention is very effective in industrial respect.

Figure 3 shows the distribution of concentration of impurities of oxygen and carbon in a semiconductor in the PIN type photoelectric transfer devices manufactured according to the method of the present invention and the conventional method. The drawing shows an aluminium back electrode 94, an N-type semiconductor, an I-type semiconductor 92, a P-type semiconductor 91 and tin oxide light transmitting conductive film 90 on the substrate, respectively.

In the exhaust method in which the exhaust system adopts a rotary pump or a mechanical booster pump only in the prior art, as a continuous exhaust system TP is not used, the carbon and oxygen contain high concentration impurity indicated by a curve 95 and a curve 96, respectively.

Especially, oxygen has 5×10^{19} ~ $2\times10^{20}cm^{-3}$ in the I-type

semiconductor 92. The drawing shows the case of containing oxygen of 5×10^{19}. In addition, due to a counterflow of oil component from a oil-sealed rotary vacuum pump, carbon contains 5×10^{20} ~ $4\times10^{20}cm^{-3}$. The drawing shows the case of containing $1\times10^{20}cm^{-3}$.

On the other hand, in the exhaust system shown in the present invention, the carbon concentration is 1×10^{17} ~ $5\times10^{18}cm^{-3}$, and generally only $1\times10^{18}cm^{-3}$ or less is contained. In addition, oxygen also contains $5\times10^{18}cm^{-3}$ or less, preferably, 1×10^{18} cm^{-3}or less, and in the Figure 2, the case of $2\times10^{18}cm^{-3}$ is shown.

In Figure 3, aluminium of the back electrode 94 has oxygen of 3 ~ $6\times10^{20}cm^{-3}$. Accordingly, it is considered that this oxygen becomes oxygen of background in the measurement of SIMS (secondary ion analyzing method) (using 3F type by CAMEKA Corp.), and oxygen in the N-type semiconductor 93 amounts to 10^{18} ~ $10^{20}cm^{-3}$.

Further, as oxygen in the P-type semiconductor and water component contained in DMS are existent, impurities are existent, and this starting material is made into oxygen of 0.1 PPM or less or an oxide by refining silane, whereby the

possibility of lowering the oxygen concentration can be estimated.

Concerning the kind of a semiconductor to be formed, not only Si, but a single layer or a multi-layer of Ge, Si_xC_{1-x} ($0<x<1$), Si_xGe_{1-x} ($0<1<x$) may be all right, and further in addition to the above, a non-oxygenation matter such as a compound semiconductor or the like such as GaAs, GaAlAs, BP, CdS or the like may be all right.

In the present invention, PCVD method in the multi-chamber system is shown using three reaction vessels. However, it is effective to reduce the number of vessels to one reaction vessel, and form silicon nitride by PCVD reaction of silane (SiH_4 or Si_2H_6) and ammonia (NH_3) by PVCD method.

A non-single crystal semiconductor film formed in the present invention is effective for N (source) I(channel forming region) N (drain) junction or PIP junction in the insulating gate type field effect semiconductor device. Further, it may be all right to make a PIN-junction type visible light laser, a light emitting element or a photoelectric transfer device of a PIN diode with an energy band width of W-N-W (wide-narrow-wide) or Si_xC_{1-x} -Si- Si_xC_{1-x} ($0<x<1$) structure. Especially, the so-called W (P or N type)-N (I-type) (wide to narrow) having the hetero junction

structure with a larger energy band width on the light incidence side can be independently manufactured with not only the conductive type but the product varied in each reaction chamber and stacked, and this is very important in industrial respect.

In the present invention, the separation part is provided with not only a gate valve but also with two gate valves and one buffer chamber as the system 2, thereby further preventing mixing of impurities of the P-type semiconductor in the I-type semiconductor layer so as to improve the characteristic.

Needless to say, the plasma CVD device of the present invention can be applied to a single chamber of the other structure or a multi-chamber system.

The embodiment of the present invention is a multi-chamber system shown in Figure 1, and in all reaction vessels, PCVD method is provided. However, at need, some or all of the vessels may adopt a photo CVD method without plasma, LT CVD method (called HOMO CVD method), or a pressure reduced CVD method to form a composite film.

4. Brief Description of the Drawings

Figures 1 and 2 show the outline of a plasma vapor phase reaction film manufacturing apparatus for embodying the present invention; and

Figure 3 shows the distribution of impurities in the semiconductor devices manufactured according to the methods of the present invention and the prior art.